TABLE 1

legacy channels and use of Walsh space

Channel	Walsh codes	Node in FIG. 5
R-FCH	W^{16}_{4}	557
R-CQICH	W^{16}_{12}	553
R-DCCH	W^{16}_{8}	563
R-PICH	W^{32}_{0}	568
R-ACKCH	W^{64}_{16}	566

Conventionally, the covering of the symbols with a Walsh code in a traffic channel would be accomplished by taking the Walsh code that is appropriate for the traffic channel and modulating the symbols with the Walsh code. The resulting data would then be transmitted on the corresponding Walsh channel. Because it is intended for the R-ESCH in the present embodiment to use Walsh resources corresponding to three quarters of the Walsh space, however, more than a single Walsh channel must be used (no single Walsh channel covers all of the desired Walsh space without also covering the already-used. Walsh space). Rather than using the Walsh codes for each of the three available quarters of the Walsh space (W^4_2, W^4_1, and W^4_3), in connection with three corresponding Walsh channels, only two Walsh channels and the corresponding Walsh codes (W^4_2 and W^2_1) are used. This is somewhat counter intuitive because it might be simpler to implement the use of Walsh codes that are all the same length (i.e., W^4_n) instead of different lengths (W^4_2 and W^2_1). The different length codes used in this embodiment, however, provide improved performance in that the use of fewer channels (two instead of three) results in a lower peak-to-average ratio.

The embodiment described utilizes three quarters of the Walsh space to cover the data transmitted over a reverse link data channel. As noted above, this embodiment may be implemented in a mobile station in a wireless communication system. An alternative embodiment may comprise a base station for receiving the data transmitted over the reverse link data channel and decoding the data. The process of decoding the data would essentially follow the reverse of the foregoing channel description. For instance, the received signal would be demultiplexed and decoded using the different-length Walsh codes to generate subpacket symbols, which would then be multiplexed into a single stream of symbols that could be decoded in a relatively conventional manner. The invention therefore includes embodiments that can be implemented with respect to both the transmission and reception of data.

Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A transmitter operable to communicate with a receiver via a wireless communication channel, wherein the transmitter comprises:

a processing subsystem: and

a transmitter subsystem coupled to the processing subsystem;

wherein the processing subsystem is configured to cover different portions of an initial data stream, each portion comprising an I/Q pair of modulated symbols and each portion being of a different quantity of modulated symbols, to be transmitted on a first wireless communication channel with at least two different-length spreading codes such that each spreading code covers each I/Q pair; and

wherein the transmitter subsystem is configured to transmit a resulting final data stream on the first wireless communication channel.

2. The transmitter of claim **1**, wherein the processing subsystem comprises a demultiplexer configured to demultiplex the initial data stream into a plurality of intermediate data streams.